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ABSTRACT

The design, development, test, and evaluation of an electronic hardware device interfacing a commercially available slide projector with a plasma panel computer terminal is reported. The interface device allows an instructional computer program to select slides for viewing based upon the lesson student situation parameters of the instructional strategy employed. Photographs and schematic drawings illustrate the interface circuitry. Appendixes cover the board layout, PROM pattern, parts list, wiring, and box connections. (Author/DS)

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AFHRL-TR-75-20

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DESIGN OF A COMPUTER-CONTROLLED, RANDOM-ACCESS SLIDE PROJECTOR INTERFACE

By

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TECHNICAL TRAINING DIVISION
Lowry Air Force Base, Colorado 80230

August 1975
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Technical Training Division

Approved for publication.

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The Technical Training Division of the Air Force Human Resources Laboratory has a research and development mission to improve Air Force training through the application of instructional and computer technology in the administration and management of individualized instruction. Within this new pedagogic environment, a computer-controlled random-access image projection capability is desired. This is a report on the successful design, development, test and evaluation of an electronic hardware device interfacing a commercially available slide projector with a plasma panel computer terminal. The interface device allows an instructional computer program to select slides for viewing based upon the lesson/student situation parameters of the instructional strategy employed.

SUMMARY

Problem

The current version of the University of Illinois PLATO IV plasma panel terminal contains a computer-controlled random-access image projection system. This system has a number of features which limit its usefulness in many environments. The two major limitations are the use of non-standard microfiche which requires a unique production capability and the use of compressed air to drive the image selector. The purpose of this effort was to develop an alternative computer-controlled projection capability using a standard off-the-shelf 35mm random-access projection system which could be interfaced to the PLATO IV plasma panel terminal.

Approach

A Kodak RA-960 slide projector was selected as the basic projection system. Interface circuitry was designed to permit the projector to be driven by the PLATO IV terminal signals. A basic consideration in the design of the interface was that no physical changes be made either to the slide projector or the computer terminal and that no computer software conversion be necessary. Standard 35mm slides were chosen as the image medium as opposed to fiche or film strip because they seemed to have many advantages for local production and courseware research and development.

Results

A highly satisfactory interface device has been built. The interface logic was built to fit on one printed circuit board (Figure 1). If the computer terminal is modified by adding a connector, with suitable power supply connections within the terminal, the printed circuit board can be inserted directly into the existing card rack of the terminal. So that no terminal modifications need be made, a "black box" (Figure 2) was designed to hold a card connector, a power supply, and the printed circuit board. The resulting interface device plugs into the terminal slide jack to pick up binary slide command information, plugs into the projector to provide it the slide selection signals, and plugs into a 110 VAC power outlet to provide power for the device.

The interface device, the slide projector, and the computer terminal (Figure 3) individually and as a system have been found to be very reliable. The unit quantity parts cost of the complete interface device currently is $148.00.

Conclusions

The developed computer-controlled random-access slide projection capability has greatly enhanced the Division's research and development capability in the application of computer technology to training and education.

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DESIGN OF A COMPUTER-CONTROLLED, RANDOM-ACCESS SLIDE PROJECTOR INTERFACE

I. INTRODUCTION

The Air Force Human Resources Laboratory (AFHRL), Technical Training Division, at Lowry Air Force Base, Colorado, has a primary mission to carry out exploratory and advanced development programs to improve the technical training of personnel in all major commands in the Air Force.

Under a sub-mission, the application of computer technology, four PLATO IV computer terminals were obtained. PLATO IV is a large-scale computer assisted instruction system being implemented by the University of Illinois. The PLATO IV terminal contains a plasma display panel which was invented by Dr Don Bitzer and others of the PLATO project. This panel is thin (about 1/4 inch) and adequately transparent, so that images can be projected onto a rear projection screen placed at the rear of the panel. The PLATO IV terminal also contains a fiche projector, which is another PLATO invention. Each fiche contains up to 256 images, each of which is 0.1 inch square. Any one of the 256 images can be randomly accessed under computer control and projected onto the rear of the plasma display.

The major problem experienced in the use of this projector is that the fiche do not meet the DOD standard for microform image size. Thus, there is a problem with availability of fiche generation equipment. Currently, the PLATO project has the only known camera system for efficient fiche production. This system uses 35mm slides as the masters for the fiche. Our experience was that, once we had the 35mm slides in hand, obtaining the fiche involved extra delay and extra cost without adding any advantages to the research and development environment of concern.

A search of commercially available projectors led to the decision to build an interface to a Kodak RA-960 slide projector The interface design requirements were that no modifications be made to the projector or the computer terminal, that no PLATO computer software slide-command changes be necessary, and that the device be highly reliable. The remainder of this report is a highly technical discussion about the theory of operation of the interface device (Figures 1 through 3).

The plasma panel terminals themselves have been found to be highly versatile and reliable. They have been adapted for use in the Air Force Advanced Instructional System (AIS). The AIS is a prototype computer-based individualized instructional system being developed by AFHRL at Lowry AFB.

II. THEORY OF OPERATION

The operation of the interface device is summarized in Figure 4. The PLATO IV TUTOR computer language has a software command called "SLIDE" with a tag designating the number of the slide to be shown; i.e., SLIDE n1. When executed this command places the binary value of n1 at the terminal slide jack accompanied by a strobe (data ready) signal. This causes the projector to select an image, to turn the lamp on and to display the desired slide. The corresponding command in the CAMIL language for the AIS is "select <slide number>," such as "select 22" or "select x+5y."

The binary number of the desired slide is latched into the interface device by a strobe signal provided by the terminal. Once latched, this binary number serves as the input data word for a programmable read-only-memory (PROM). The PROM allows conversion of this binary number to its equivalent base 9 value, since base 9 is required by the Kodak RA-960 projector.

The new base 9 number then serves as the input address for the interface device high and low order decoder/demultiplexors. Eighteen address lines (9 high order and 9 low order) from the decoders are buffered through drivers and protective diodes. These lines then lead to the projector.

During the entire slide selection process there are three critical timing sequences for successful operation and reliability:

1. The Lamp on/off data line from the terminal is delayed until the slide number data lines have settled and have been latched. Then, this on/off data line activates an interface relay which controls the on/off operation of the slide projector.

2. When the interface relay turns the projector on, as discussed above, a tremendous amount of electromechanical noise is created by its motors and relays. Another delay is created to allow this noise to decay. Then an "initiate-access" signal is sent to the projector which causes the projector to seek out the appropriate slide position.

3. During the projector search mode, the high order digit (multiples of nine) of the slide number is sought first. Once the slide tray sector corresponding to this high order digit is found, the projector sends a "low order enable" signal back to the interface device. The interface device must not provide the low order digit (multiples of one) until the "low order enable" signal is received.

The circuit schematic for the complete device is shown in Figure 5. Appendixes A through E are provided as supplemental data for the construction of the interface device.

III. DISCUSSION

Software Command

The random access slide selection process is initiated with a slide selection command accompanied by an arithmetic expression for the desired slide number. To turn the projector off in TUTOR, a new slide command is given with an expression whose value is greater than 511 and less than 1024. In CAMIL the command is "select lamp off."

As a student progresses through a lesson, the computer software allows the student's responses to be used for selecting an appropriate slide or slide sequence and for controlling the display duration.

Data Strobed and Latched

When the SLIDE command is executed, a 10-bit binary value of the SLIDE variable is presented at the terminal output jack, J29. The first eight bits, called D_1 through D_8, are for slide numbers 0 to 255. (Refer to the terminal's data lines of Figure 6.) Bit 10 at D_{10} is for numbers between 511 and 1024 for control of the projector on/off state. Pin 17 of the terminal jack, J29, is the "data ready" strobe. The slide data appears on lines D_1–D_8 and D_{10} for 16.6 milliseconds. Two microseconds after the data appears, the "data ready" strobe appears and lasts for two microseconds (Refer to the Timing Diagram, Figure 7).

When the interface device receives the strobe signal from the terminal, it reconditions the wave-form by passing it through a nand gate inverter of U4, an RC ramp filter (R_3, C_3, R_2) and another nand gate inverter of U4 (Figure 5). This conditioning filters out high frequency pulses created by external noise and eliminates false clocking of the interface latches–U1 and U2. This reshaped strobe signal is the clock strobe for two 4-bit D latches, U1 and U2 (SN7475). These latches capture the binary slide number as the reshaped clock signal transitions to its low state. After being present for a total of four microseconds, data lines D_1–D_8 are latched onto the interface board, but D_{10}, the projector on/off signal, has not yet been processed.

Slide Projector On/Off

After the binary slide number data has been latched, D_{10} is still present. When the reshaped "data ready" strobe triggers the slide number latching, it also triggers a 20 microsecond one-shot delay pulse at U5. This delay is created to insure that the on/off operation of the projector occurs only after the address data is securely latched. After this delay, a second one-shot in U5 is fired to produce a pulse which latches the on/off data (D_{10}) into U6. This second pulse is very short (3.5 microseconds) to insure a secure latching before the slide projector relay turns on (Figure 8).

After the desired on/off state is latched into U6, the interface relay S1, which controls the on/off state of the slide projector, has a renewed status. When the Q output (pin 6 of U6) is low (logic zero) it sinks current from the relay coil of S1; this energizes S1, closes its contacts, and turns the slide projector on. When Q is high (logic one) no current passes through the relay, the contacts are open and the projector is off. Thus, the projector turns on or off as Q goes low or high, respectively, and this action is based upon the delayed input signal of D_{10}.

PROM Data Conversion

At this point, the latched address data is an eight bit binary value of the desired slide. The Kodak RA-960 electromechanical addressing mechanism uses a base 9 numbering system. As the slide tray rotates, wipers contact encoded addresses at each position. The addresses are encoded based on counting by nines; i.e., 0, 1, 2, 3 . . 7, 8, 10, 11, 12 . . . 18, 20, 21 . . .

To convert the binary (base 2) to a base 9 number, an Intel C 1702A Programmable Read Only Memory (PROM), U3, is used. The PROM is arranged in an eight bit per word by 256 word matrix. An eight bit address is used to select one of the 256 words ($2^8 = 256$). The PROM used is a static one in which the output follows the input with no clocking or read/write control signals necessary. After $D_1 - D_8$ are latched, they become the eight bit binary input address for the PROM, and the PROM's output is the eight bit base 9 number used by the projector.

It should be noted that the terminal hardware was designed for up to 256 fiche images. The PROM was programmed to accommodate 256 slide number conversions but the RA-960 projector tray has only 81 slide positions As such, a slide 82 command will cause the projector to display slide 0. Of course, the interface device can be used in conjunction with several slide trays.

Decoders/Demultiplexers

It is necessary to decode the base 9 slide number into eighteen address/driver lines for the projector. These are divided into nine high order lines for the multiples of nine and nine low order lines for the multiples of one (Figures 5 and 6). The eight bit PROM output has the lower four bits coded for the low order, and the higher four bits for the high order. U7 and U8, the decoders/demultiplexers used, are SN74154 integrated circuits which have a four-bit input and a 16 line output. As will be explained in the section on high and low order slide addressing, the SN74154 is used as opposed to an SN7442 even though only 9 of the 16 lines are used.

Projector Data Line Drivers

There are now 18 address lines with the proper address pattern available to the projector. These lines, however, have transistor-transistor-logic (TTL) five volt levels which are incompatible with the control signal voltage levels required by the projector. Three SN7406 (U9, U10, and U11) hex inverter buffers/drivers are used with open collector high-voltage outputs to provide the voltage conversion required.

Diodes CR_4 to CR_{21} are required to protect the inverters. The internal addressing mechanism of the projector causes one address line to be shorted to an adjacent line. This shorting causes the high voltage signal of one line to appear on another line. The diode prevents this signal from reaching and harming the driver. There is a manually operated switch at the back of the projector for switching from the automatic random selection mode to the tray release mode. The tray releases from the projector at slide position zero. Thus, when the switch is set for tray release mode, the address lines for zero are set high. This also causes the rotation and the shorting process just described.

Initiate Slide Access

Now that the address lines are properly set for the projector, an "initiate access" signal can be sent to the projector. This signal is sent through a single-pole, single throw relay, S2, of the interface. When closed, S2 energizes a double pole, single throw relay inside the projector that controls the projector lamp and motor.

Relay S2 is controlled by U12, an SN74123. While the slide command data is being latched, converted, decoded and buffered, a 15 millisecond pause is incurred by U12. This allows all the necessary operations to occur and allows the address lines to settle after the projector has been turned on. After 15 milliseconds the second half of U12 fires and its Q output turns S2 on for 500 milliseconds. This provides the necessary "initiate access" pulse to the projector (Figure 9). The slide projector now starts its electro-mechanical search mode, rotating in the shortest direction to the requested slide.

High and Low Order Slide Addressing

When the projector starts its rotation, it first seeks that segment of the tray that represents the nine's order of the addressed slide. For successful operation, it is necessary that at this time only one high order

address line from the interface device to the projector be high while all nine low order lines are low. Thus U8, the high order decoder, must be enabled while U7, the low order decoder, is disabled during the high order search mode.

Once the tray has rotated to the correct nine's sector, the projector sends a "low order enable" signal to the interface device. This signal enables U7 for the low order search. Since the low order enable signal is not TTL compatible, it is conditioned prior to arriving at U7 by Q1, (a switching transistor) and R6 and R7. The collector output of Q1 provides the necessary voltages for TTL input conditions of "1" and "0."

It might be more efficient to use an SN7442 decoder with 10 decoded outputs, especially since only nine are used. However, the SN74154 is the only decoder with an enable/disable G input. Because of the high and then low order search sequence, this enable/disable input was required. When enabled, the four bit binary input is decoded into 16 mutually exclusive outputs with one active low. When disabled, the sixteen output lines are inactive high.

At the end of the access operation, the high order and the low order search have been completed, the correct slide is dropped from the tray for viewing, and the projector automatically adjusts the focus for proper viewing.

Power Supplies

For operation of the interface device, three voltage supplies are necessary: +5, +15, and −9. The 5 volt supply is necessary for the TTL circuits and is available from the terminal's power supply at the slide connecter jack, J29. The terminal's 5 volt supply is more than adequate to supply current for both the interface device and the terminal.

The design for the three SN7406 open collector drivers, U9, U10, and U11, requires a 15 volt supply. A 24 VDC source is obtained from the projector and dropped to 15 volts by regulator VR1 and capacitors C17 and C15. The regulator voltage drop from about 24 to 15 volts requires proper heat-sinking to protect the regulator by dissipating the power loss.

The third voltage, −9 volts, is required for the Intel PROM. The terminal has a −12 volt supply available at the card rack wiring plane. The "black box" (Figure 3) also provides a −12 volt supply which is converted on the board to −9 volts. If the interface printed circuit board is plugged directly into the card rack of the terminal, no separate power supply is required. Since the parts cost for the −12 to −9 volt conversion is minimal by using the 9 volt zener diode circuit, it was decided to use a −12 volt (instead of −9 volt) power supply inside the "black box" so that one board design would suffice for use in either the terminal card rack or in the "black box."

Reliability, Acceptance and Use

Several steps were taken to ensure ultra-high reliability. As described earlier, a small delay was created after latching the data to allow the circuitry to settle down from injected violent electrical noise created by turning the projector on. The "data ready" strobe from the projector to the interface board underwent a reshaping process to eliminate any sharp noise spikes which would cause false clocking. All integrated circuits in the strobe chain of events have by-pass capacitors (0.005 microfarads). These include U4, U5, U6, and U12. Relay S1 has an RC circuit across its contacts to supress arcing and both relays utilize diodes across their coils to supress inductively caused voltage spikes. All components used have intrinsically high levels of reliability, and all components operate well within their ratings.

An acceptance test of the terminal, interface and projector was administered for over 5,000 slide projector operations using TUTOR software. The result was that no failures were experienced by either the projector or interface device and that the only errors that occurred were attributable to the 1,000 mile data link to the central computer. These results are considered to exceed MTBF requirements for classroom use.

To use this capability for rear projection on the plasma panel display the following rearrangement was made of externally mounted terminal components. These changes were necessary to obtain an unobstructed light path. First, the fiche projector was removed from the top of the terminal. Next the air fans and their mounting panel were removed from the rear of the terminal. Then the front surface mirrors were removed from the base of the terminal. Finally, the fans were remounted on the top of the terminal. The slide projector was mounted behind the terminal such that the focal length from the projector to the glass panel was 29 inches for either a straight or folded (using a mirror) focal path. The three inch lens provided with the projector gave the proper image size at this distance.

IV. CONCLUSION

A highly reliable device has been developed to interface a Kodak RA-960 random-access slide projector with a plasma panel computer terminal. The interface device, the slide projector, and the computer terminal individually and collectively have been very reliable.

The device was designed to be used as a "black box" (Figure 2) that plugs into the terminal and projector; used in this mode no electrical modifications are needed to either the terminal or projector. The interface logic is all on one printed circuit board (Figure 1). If the terminal is modified by adding a connector and by obtaining a −12 volt supply from the back plane, then this board can be inserted directly into the terminal's existing card rack.

The computer-controlled random-access slide projector capability has greatly enhanced the research and development capability of the division. Use of slides has been found to be beneficial in research and development of courseware, where fast turn-around of a single image is desirable. In this situation, and in comparison with fiche or film strip, slides have been found to have advantages of high modularity, low unit cost, local production, short turn around time, and availability of highly reliable projection devices. For operational use of validated and relatively stable courseware, however, fiche and film strip often have advantages over slides.

Apparently many others agree that there are advantages to this capability as several requests for the device have been received from Air Force, Army and Navy organizations, as well as from civilian institutions.

Devices of this type would be much simpler if projectors were designed for TTL interfaces.

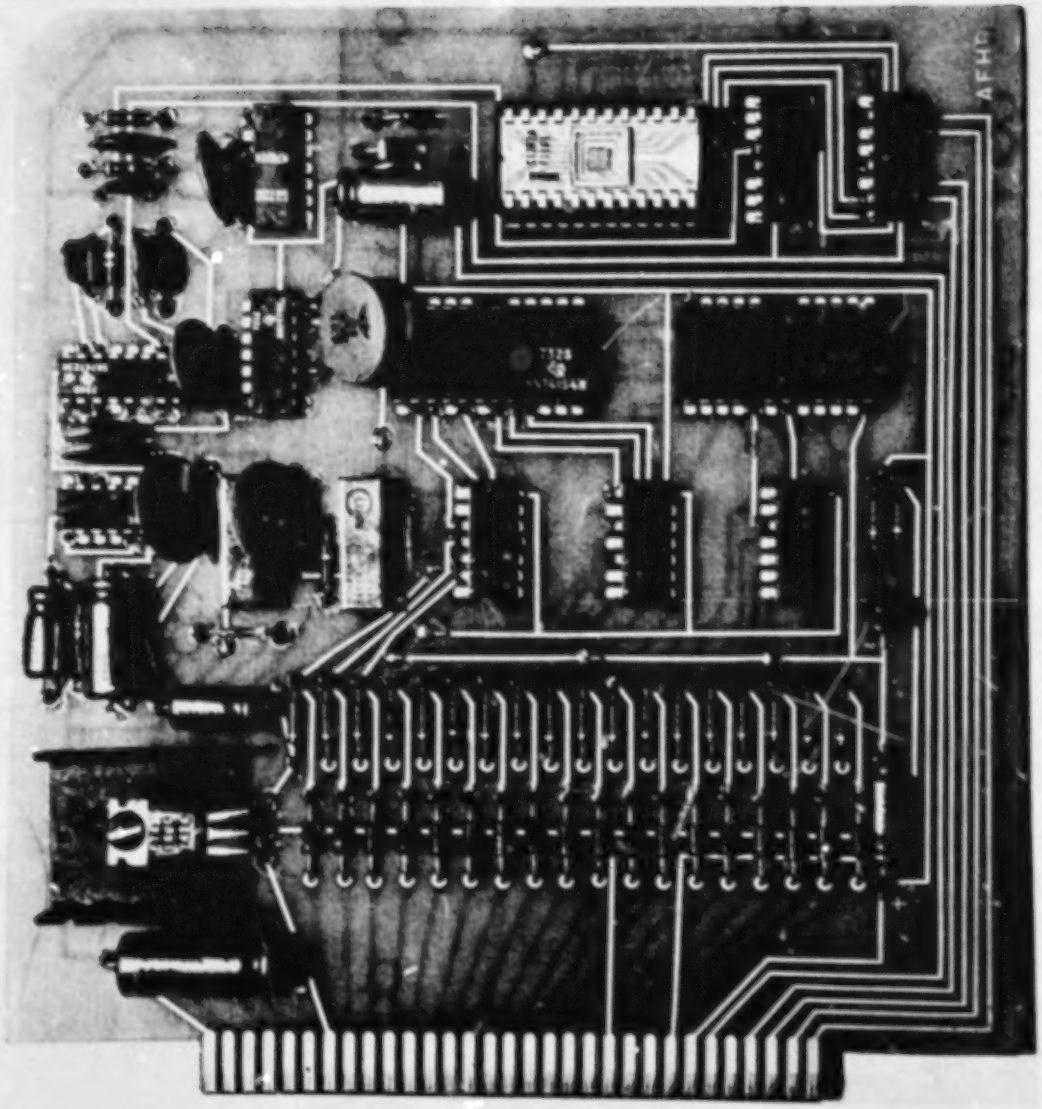


Figure 1. Interface board.

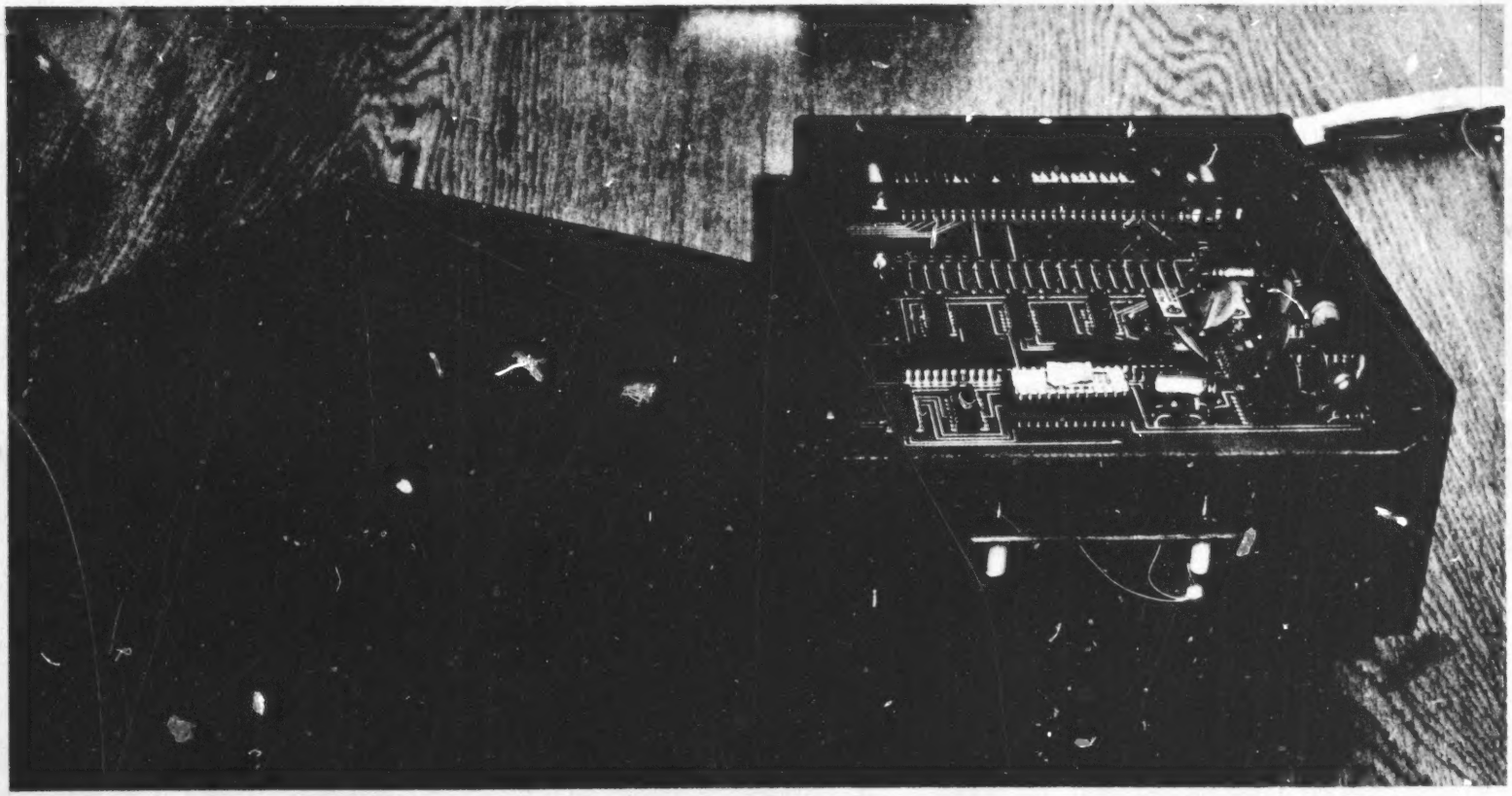


Figure 2. **Interface "black box."**

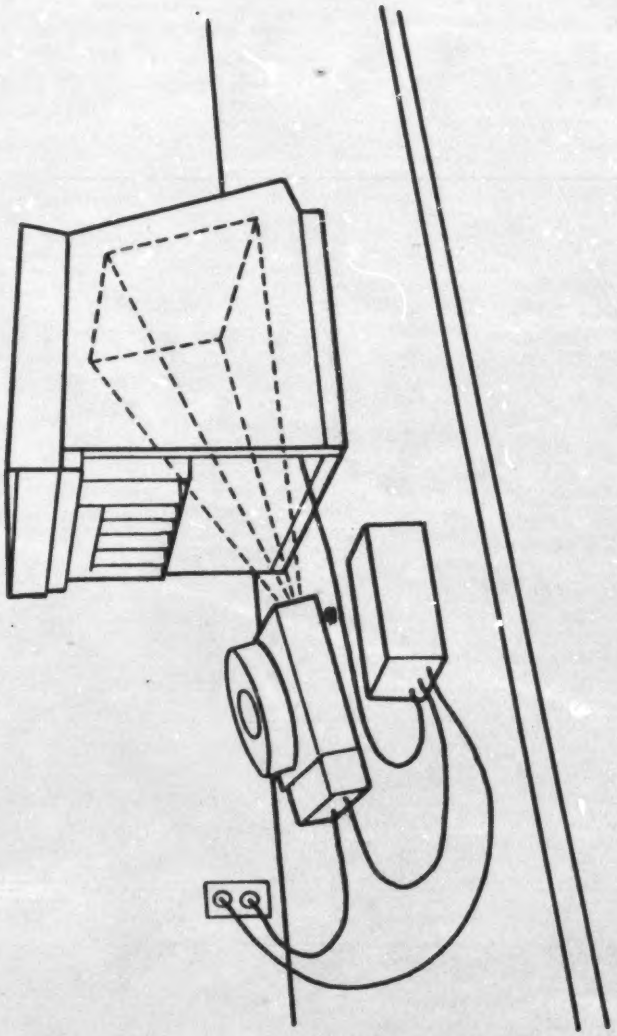


Figure 3. **Arrangement of terminal/interface/projector.**

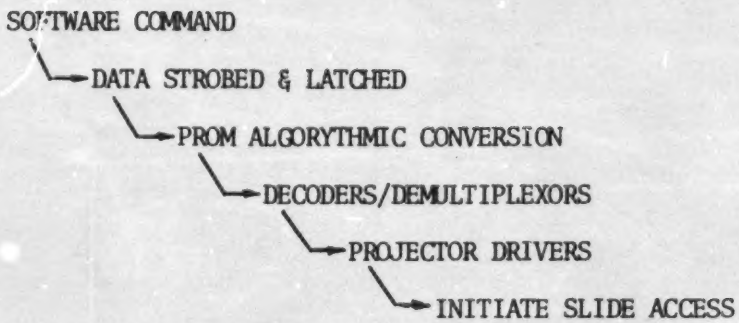


Figure 4. **Steps of operation.**

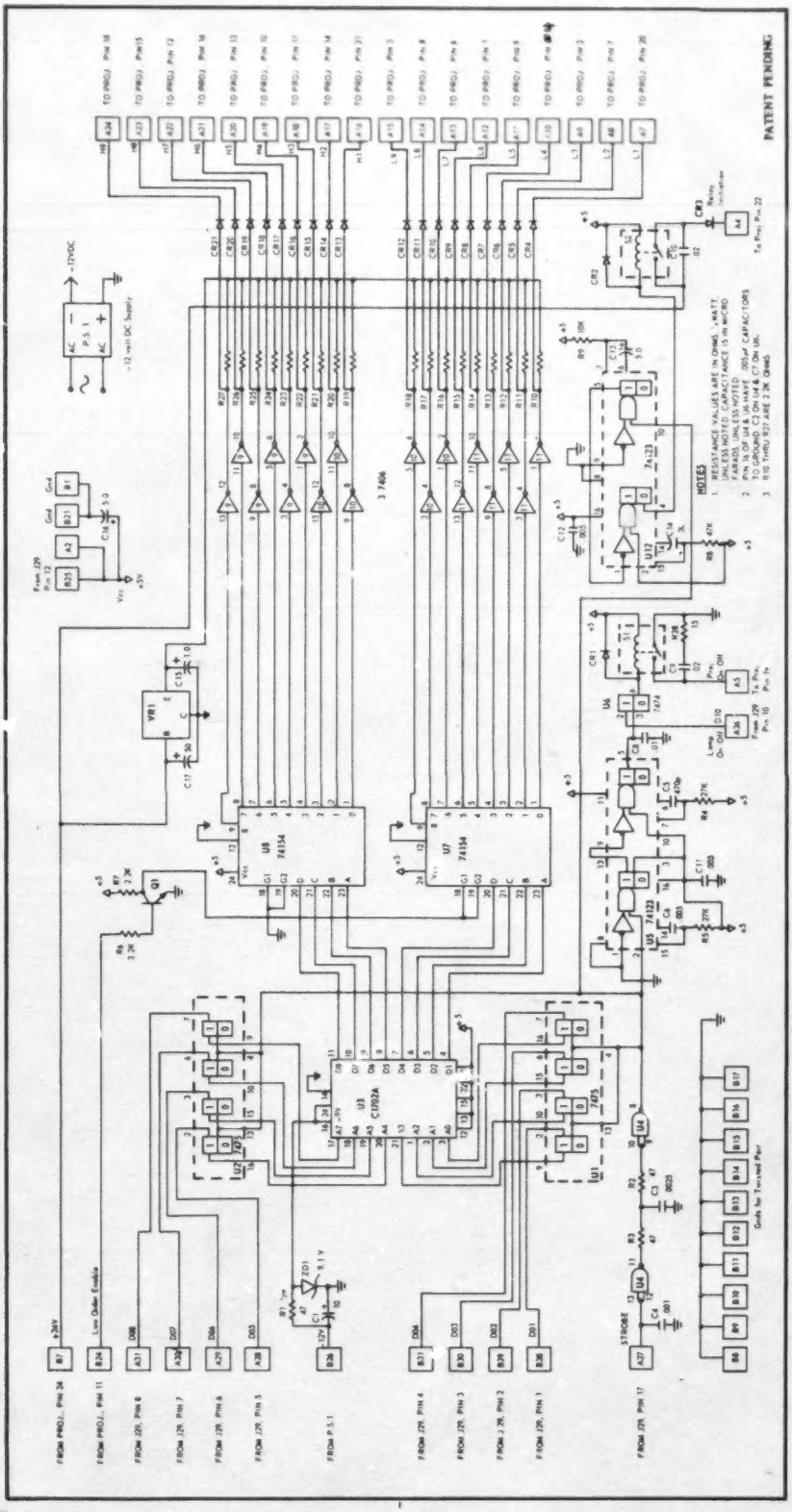


Figure 5. Schematic of interface.

From Terminal:	D_1			(least significant bit)
	D_2			
	D_3			
	D_4			
	D_5			
	D_6			
	D_7			
	D_8			(most significant bit)
	D_9			(not used)
	D_{10}			(projector on/off bit)
	Data Ready Strobe			
	+5VDC			
	Gnd			
To Projector:	L_1		H_1	
	L_2		H_2	
	L_3		H_3	
	L_4	Low Order	H_4	High Order
	L_5	Slide Selection	H_5	Slide Selection
	L_6		H_6	
	L_7		H_7	
	L_8		H_8	
	L_9		H_9	
	Relay Initiation Pulse			
	Projector On/Off Line			
From Projector:	Low Order Enable Line			
	+24VDC			
	Gnd			
To Interface Board:	−12 VDC Power Supply			
	Gnd			

Figure 6. **Interfacing data lines.**

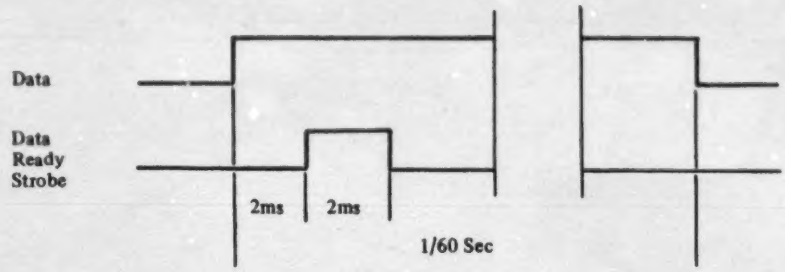


Figure 7. **Timing diagram – computer terminal slide jack output.**

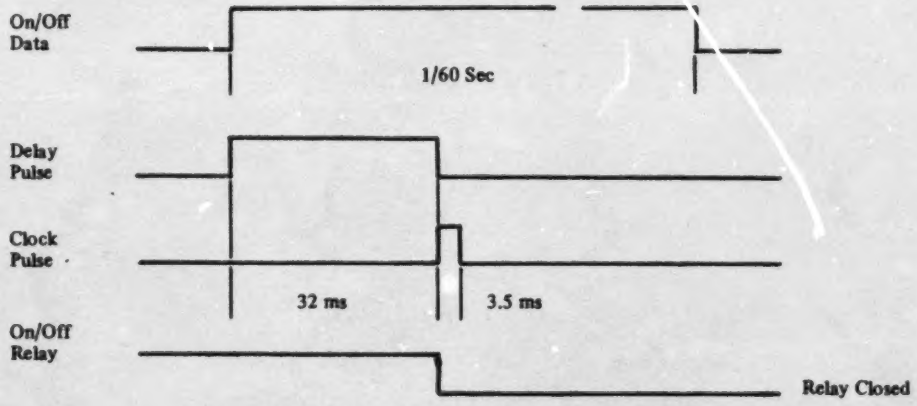


Figure 8. **Timing diagram – projector on/off relay.**

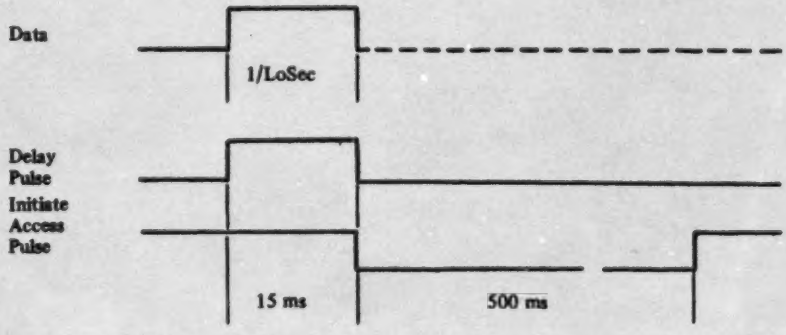
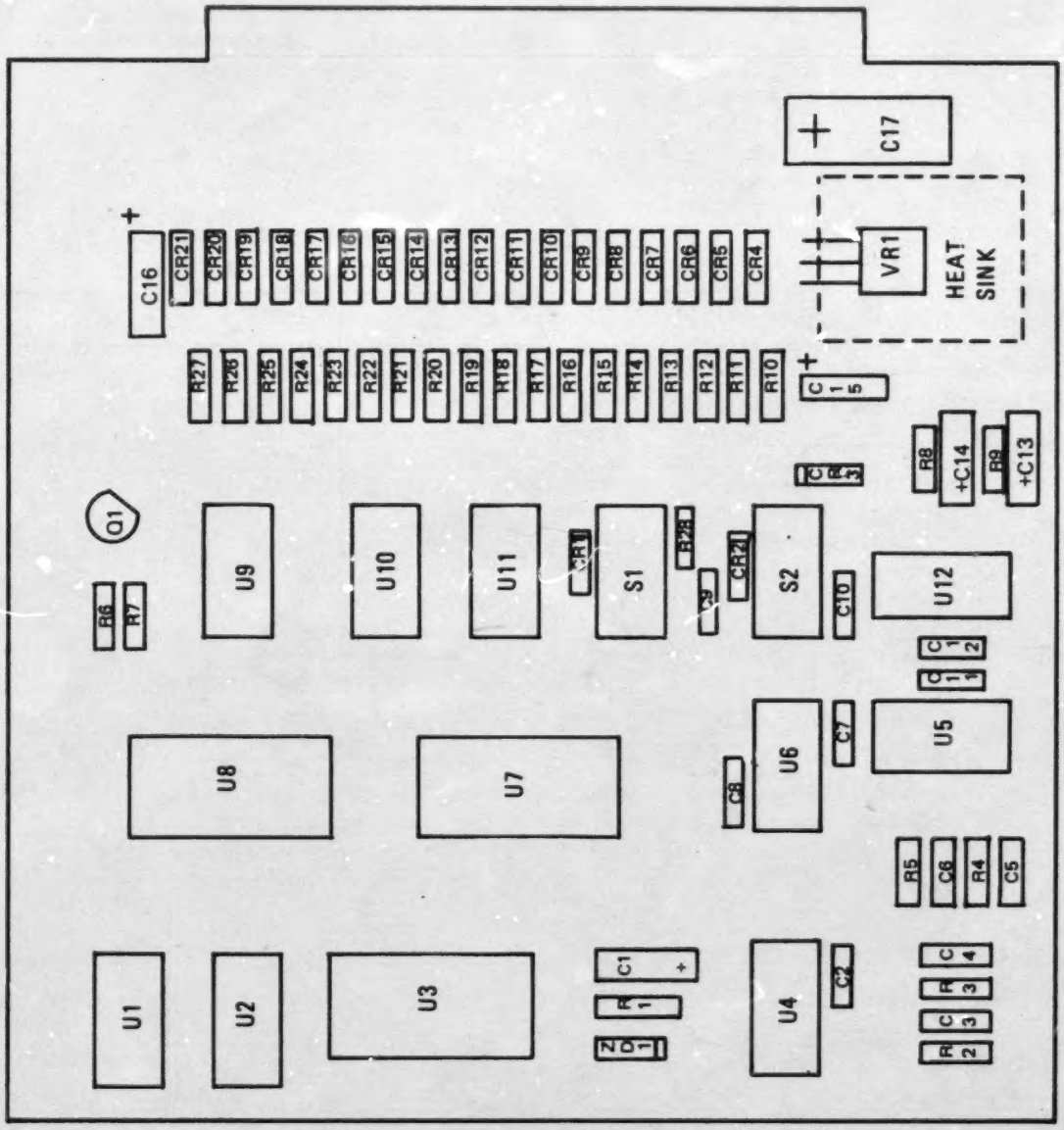


Figure 9. **Timing diagram – initiate access pulse to projector.**

APPENDIX A: BOARD LAYOUT



PLATO/PROJECTOR INTERFACE BOARD
COMPONENT LOCATION

APPENDIX B: PROM PATTERN

Word Address:	PROJECTOR/INTERFACE PROM MASK Octal Bit Pattern							
032 000	000:	001:	002:	003:	004:	005:	006:	007:
032 010	010:	020:	021:	022:	023:	024:	025:	026:
032 020	027:	030:	040:	041:	042:	043:	044:	045:
032 030	046:	047:	050:	060:	061:	062:	063:	064:
032 040	065:	066:	067:	070:	100:	101:	102:	103:
032 050	104:	105:	106:	107:	110:	120:	121:	122:
032 060	123:	124:	125:	126:	127:	130:	140:	141:
032 070	142:	143:	144:	145:	146:	147:	150:	160:
032 100	161:	162:	163:	164:	165:	166:	167:	170:
032 110	200:	201:	202:	203:	204:	205:	206:	207:
032 120	210:	000:	001:	002:	003:	004:	005:	006:
032 130	007:	010:	020:	021:	022:	023:	024:	025:
032 140	026:	027:	030:	040:	041:	042:	043:	044:
032 150	045:	046:	047:	050:	060:	061:	062:	063:
032 160	064:	065:	066:	067:	070:	100:	101:	102:
032 170	103:	104:	105:	106:	107:	110:	120:	121:
032 200	122:	123:	124:	125:	126:	127:	130:	140:
032 210	141:	142:	143:	144:	145:	146:	147:	150:
032 220	160:	161:	162:	163:	164:	165:	166:	167:
032 230	170:	200:	201:	202:	203:	204:	205:	206:
032 240	207:	210:	000:	001:	002:	003:	004:	005:
032 250	006:	007:	010:	020:	021:	022:	023:	024:
032 260	025:	026:	027:	030:	040:	041:	042:	043:
032 270	044:	045:	046:	047:	050:	060:	061:	062:
032 300	063:	064:	065:	066:	067:	070:	100:	101:
032 310	102:	103:	104:	105:	106:	107:	110:	120:
032 320	121:	122:	123:	124:	125:	126:	127:	130:
032 330	140:	141:	142:	143:	144:	145:	146:	147:
032 340	150:	160:	161:	162:	163:	164:	165:	166:
032 350	167:	170:	200:	201:	202:	203:	204:	205:
032 360	206:	207:	210:	000:	001:	002:	003:	004:
032 370	005:	006:	007:	010:	020:	021:	022:	023:

APPENDIX C: PARTS LIST

Reference Designation				
C1	10 microfarad	50 volts	Electrolytic	Capacitor
C2	.005 microfarad		Ceramic	Capacitor
C3	.0025 microfarad		Ceramic	Capacitor
C4	.001 microfarad		Ceramic	Capacitor
C5	470 picofarad		Ceramic	Capacitor
C6	.005 microfarad		Ceramic	Capacitor
C7	.005 microfarad		Ceramic	Capacitor
C8	.01 microfarad		Ceramic	Capacitor
C9	.02 microfarad		Ceramic	Capacitor
C10	.02 microfarad		Ceramic	Capacitor
C11	.005 microfarad		Ceramic	Capacitor
C12	.005 microfarad		Ceramic	Capacitor
C13	5 microfarad	16 volts	Electrolytic	Capacitor
C14	30 microfarad	16 volts	Electrolytic	Capacitor
C15	1 microfarad	50 volts	Electrolytic	Capacitor
C16	5 microfarad	16 volts	Electrolytic	Capacitor
C17	50 microfarad	50 volts	Electrolytic	Capacitor

CR1 thru CR3	1N4148	Switching Diode
CR4 thru CR21	1N4002	Silicon Rectifier Diode

P.S. 1	Power Supply, 110 volts a.c. to 12 volts d.c., 120 ma. Wanlass Model TW12-120	
Q1	2N3565	NON Transistor

R1	47 ohm	Resistor ± 5%	1/2 watt
R2-R3	47 ohm	Resistor ± 10%	1/4 watt
R4-R5	27K ohm	Resistor ± 10%	1/4 watt
R6-R7	2.2K ohm	Resistor ± 10%	1/4 watt
R8	47K ohm	Resistor ± 10%	1/4 watt
R9	10K ohm	Resistor ± 10%	1/4 watt
R10-R27	2.2K ohm	Resistor ± 10%	1/4 watt
R28	15 ohm	Resistor ± 10%	1/4 watt

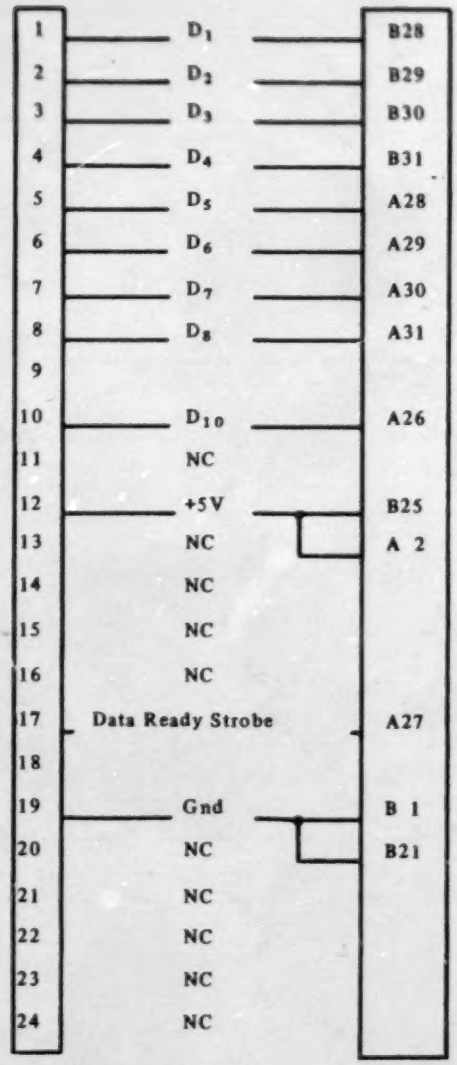
S_1, S_2		CLARE REED Relays, Part No. PRB 3510
U1-U2	SN7475N	Integrated Circuit
U3	Intel C1702A	Integrated Circuit
U4	SN7400N	Integrated Circuit
U5,U12	SN7412N	Integrated Circuit
U6	SN7474N	Integrated Circuit
U7-U8	SN7415N	Integrated Circuit
U9,U10,U11	SN7405N	Integrated Circuit

Reference Designation		
VR1	15 volt Voltage Regulator	Fairchild μGH7815
ZD1	9.1 volt	Zener Diode

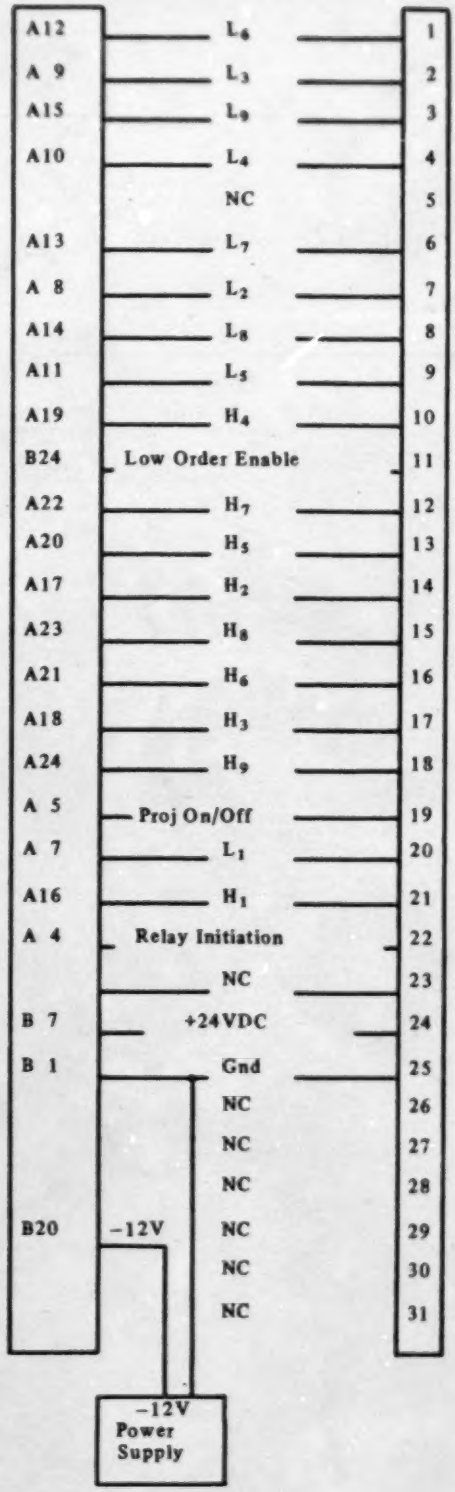
Miscellaneous Items

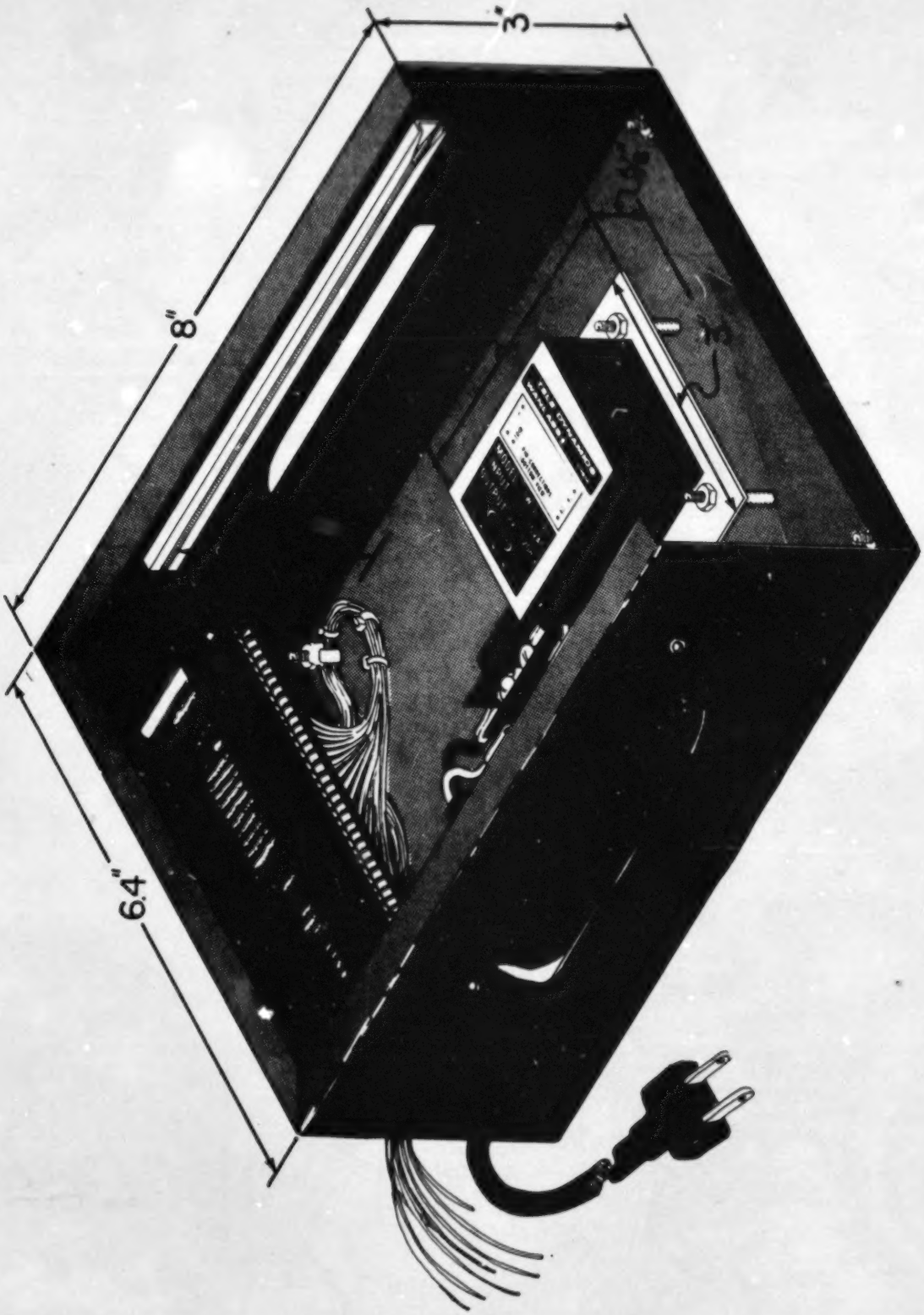
Card Edge Connector	Mfr'd by AMP, 31/62 pin #67467-8
Heat Sink	Mfr'd by IERC, #PB1-2B, Hole pattern #2
PROM Socket	24 pin dual-In-Line I.C. Socket
Cable connector plug	Amphenol, Series 222, "Mightly Mite," #222-11N31
Contacts for above plug	Amphenol, "Wire Form" #220-P01
Card Guide	Scanby, Snap-In Type, #23071-5
Terminal Block	2-Contact Type, Cinch Series Type 2-141
Connector (Terminal Jack 29)	AMP

APPENDIX D. WIRING CONNECTIONS



NOTE: All data lines between the terminal and the interface board must be twisted pair.





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